A Balanced Wideband VCO for Set-Top TV Tuner Applications

Alpha

APN1005

Introduction

Modern set-top TV DBS tuner systems require more channel coverage, while maintaining competitive prices. This situation creates tough design goals: to improve performance and simplify design.

Balanced VCO configuration could be a competitive circuit solution, since it provides the widest tuning range with practical circuitry and layout. However, tuning margins would be further improved by optimizing the varactor manufacturing process. Alpha Industries has developed such a process to satisfy the most ambitious wideband design goals.

In this publication, we will address the design of the balanced-type voltage control oscillator (VCO) based on the newly developed varactor SMV1265-011 with the unique set of capacitance tuning ratios and Q-quality.

VCO Model

Figure 1 shows the VCO model built for open loop analysis in Libra Series IV including the SMV1265-011 varactor model.

The circuit schematic in Figure 2 shows a pair of transistors in a single feedback loop, connected so that collector currents would be 180° shifted (ideally). A pair of back-to-back connected SMV1265-011 varactors is used, rather than a single one. This allows lower capacitance at the high voltage range, without changing the tuning ratio. The reason is that apart from package capacitance, certain mounting fringing capacitances, though small, may strongly affect higher frequency margins. The effects of parasitic capacitances were summarized in the model as C_4 and C_3, valued 0.4 pF each. These values may vary depending on the layout of the board. Varactor DC biasing is provided through resistors R_6 and R_8, both 1 k, which may affect the phase noise, but eliminate the need for inductive chokes. This minimizes overall costs and the possibility of parasitic resonances — the usual cause for frequency instability and spurs.

The phase corrector DC chokes, SRL_1 and SRL_2, were modeled as lossless inductors at 33 nH since their losses are dominated by the 30 Ω emitter biasing resistors. DC blocking series capacitances (C_{SER1} and C_{SER2}) are modeled as an SRC network, including associated parasitics. Their values were optimized to 10 pF providing smooth tuning over the design band.

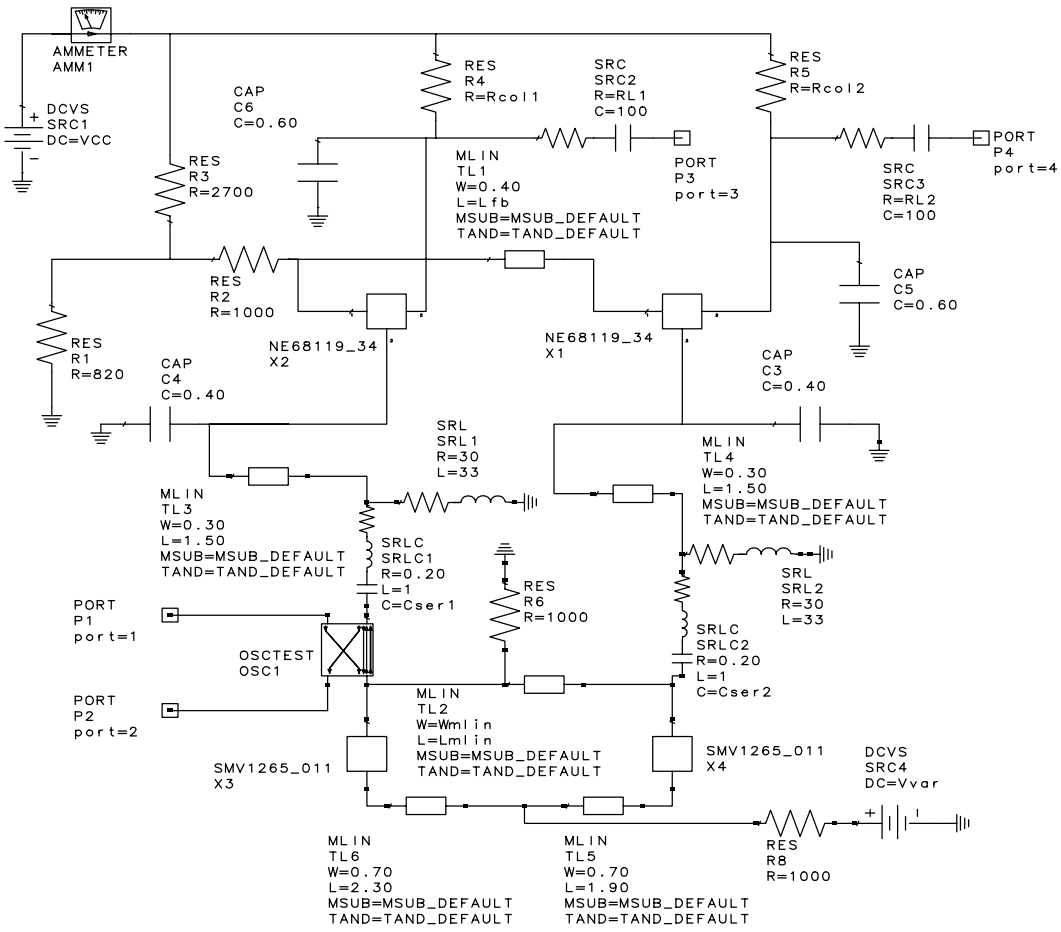

Figure 1. VCO Model, Including SMV1265-011 Varactor Model

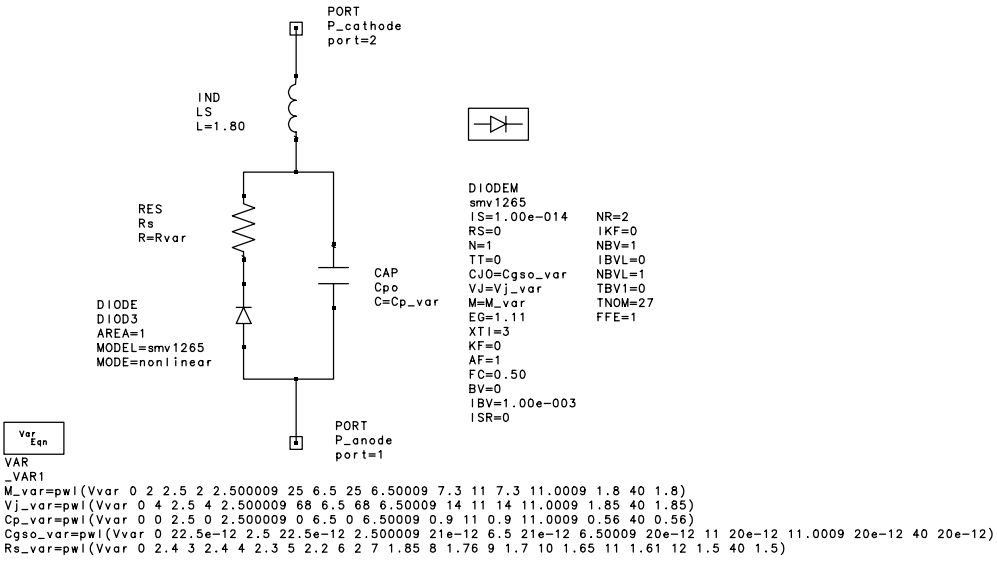

Figure 2. Transistor Pair in Single Feedback Loop

The pseudo-resonator inductance is formed by microstrip transmission line TL_2, which provides necessary circuit response at high frequencies. This has little effect at the lower band due to the resonator's dominantly capacitive nature.

The function of transmission line TL_1 is both feedback and phase alignment — providing flat power response over the tuning range.

Power output is supplied from the collectors of X_1 or X_2 through the series connected resistance and DC blocking capacitance SRC_2 and SRC_3.

DC biasing for both of the transistors is supplied through a resistive divider $R_1/R_3/R_2$.

The NEC NE68119 bipolar transistors were selected to best fit performances. Note: The circuit is very sensitive to the transistor choice (in terms of tuning range and stability) due to wide bandwidth design requirements.

For the model of NEC NE68119 we used the Gumel Poon model of Libra IV with the coefficients provided by CEL RF & Microwave Semiconductors Catalogue, 1997-98.

In the Libra test bench shown in Figure 3 we defined an open loop gain ($Ku = V_{OUT}/V_{IN}$) as the ratio of voltage phasors at the input and output ports of an OSCTEST component. Defining the oscillation point requires the balancing of input (loop) power to provide zero gain for a zero loop phase shift. Once the oscillation point is defined the frequency and output power can be measured. Use of the OSCTEST2 component for the close loop analysis is not recommended, since it may fail to converge in some cases, and doesn't allow clear insight into the understanding of VCO behavior. This property is considered an advantage of modeling over a purely experimental study.

In the default bench shown in Figure 4 the variables used for more convenient tuning during performance analysis and optimization are listed in a "variables and equations" component.

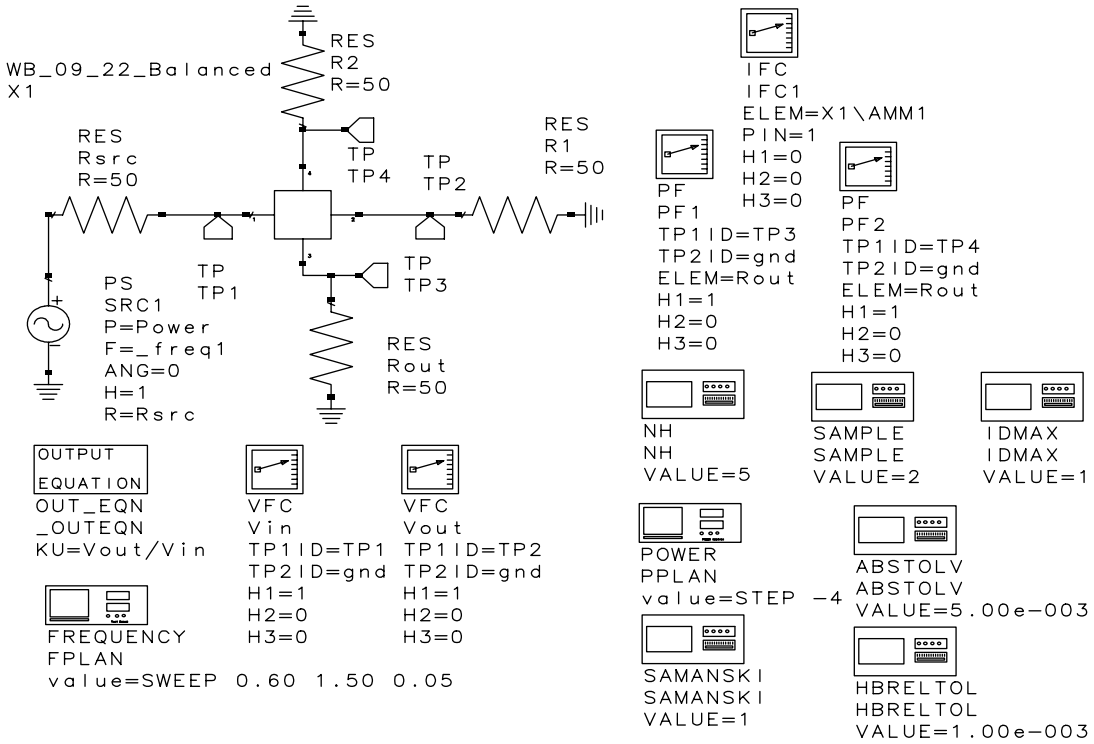

Figure 3. Libra Test Bench

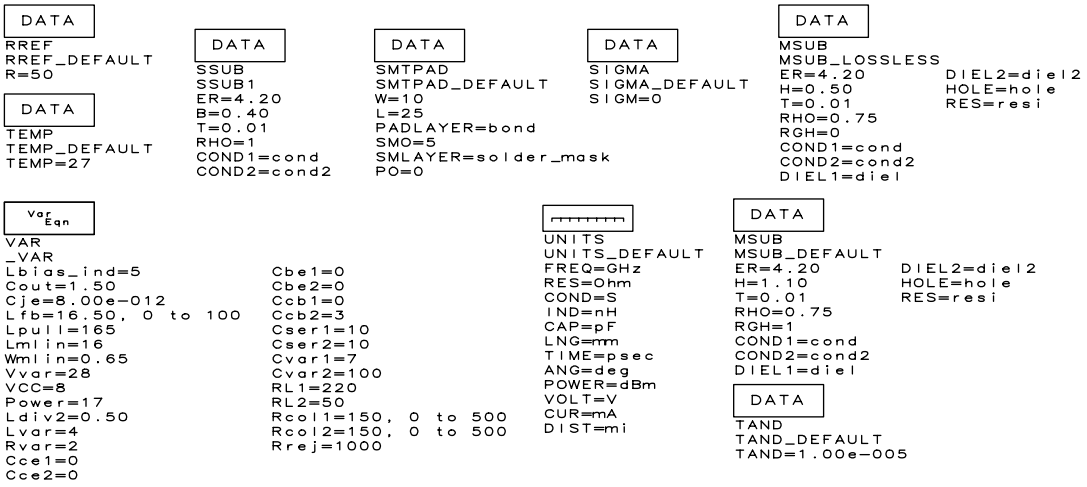

Figure 4. Default Bench

SMV1265-011 SPICE Model

Figure 5 shows a SPICE model for the SMV1265-011 varactor diode, defined for the Libra IV environment, with a description of the parameters employed.

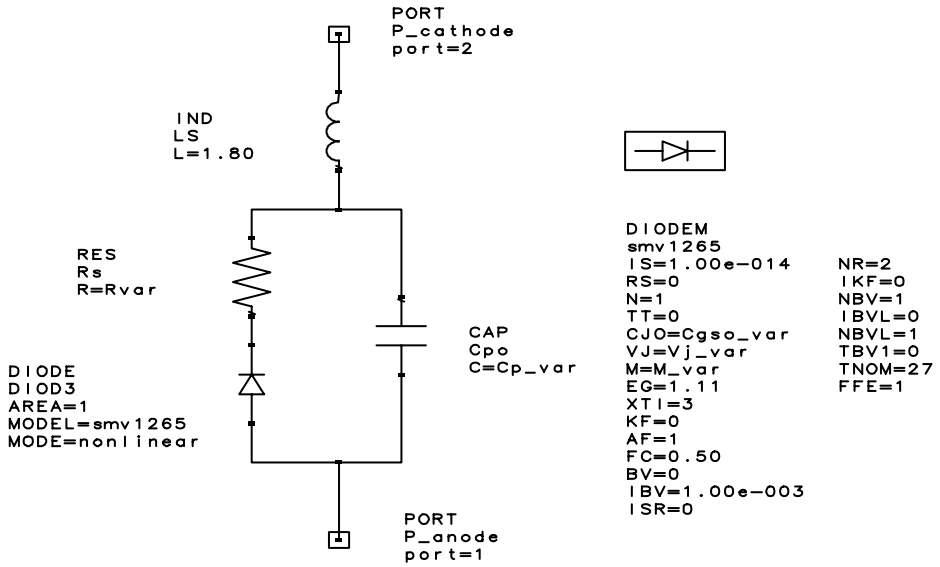

Figure 5. SMV1265-011 Libra IV SPICE Model

Parameter	Description	Unit	Default
IS	Saturation current (with N, determine the DC characteristics of the diode)	A	1e-14
R_S	Series resistance	Ω	0
N	Emission coefficient (with IS, determines the DC characteristics of the diode)	-	1
TT	Transit time	S	0
C_{JO}	Zero-bias junction capacitance (with V_J and M, defines nonlinear junction capacitance of the diode)	F	0
V_J	Junction potential (with V_J and M, defines nonlinear junction capacitance of the diode)	V	1
M	Grading coefficient (with V_J and M, defines nonlinear junction capacitance of the diode)	-	0.5
E_G	Energy gap (with XTI, helps define the dependence of IS on temperature)	EV	1.11
XTI	Saturation current temperature exponent (with E_G, helps define the dependence of IS on temperature)	-	3
KF	Flicker noise coefficient	-	0
AF	Flicker noise exponent	-	1
FC	Forward-bias depletion capacitance coefficient	-	0.5
B_V	Reverse breakdown voltage	V	Infinity
I_{BV}	Current at reverse breakdown voltage	A	1e-3
ISR	Recombination current parameter	A	0
NR	Emission coefficient for ISR	-	2
IKF	High-injection knee current	A	Infinity
NBV	Reverse breakdown ideality factor	-	1
IBVL	Low-level reverse breakdown knee current	A	0
NBVL	Low-level reverse breakdown ideality factor	-	1
T_{NOM}	Nominal ambient temperature at which these model parameters were derived	°C	27
FFE	Flicker noise frequency exponent		1

Table 1. Silicon Varactor Diode Default Values

Table 1 describes the model parameters. It shows default values appropriate for silicon varactor diodes which may be used by the Libra IV simulator.

According to the SPICE model in Figure 4, the varactor capacitance (C_V) is a function of the applied reverse DC voltage (V_R) and may be expressed as follows:

$$C_V = \frac{C_{JO}}{\left(1 + \frac{V_R}{V_J}\right)^M} + C_P$$

This equation is a mathematical expression of the capacitance characteristic. The model is accurate for abrupt junction varactors (Alpha's SMV1400 series); however, the model is less accurate for hyperabrupt junction varactors because the coefficients are dependent on the applied voltage. To make the equation fit the hyperabrupt performances for the SMV1265-011 a piece-wise approach was employed. Here the coefficients (V_J, M, C_{JO}, and C_P) are made piece-wise functions of the varactor DC voltage applied. Thus, the whole range of the usable varactor voltages is segmented into a number of subranges each with a unique set of the V_J, M, C_{JO}, and C_P parameters as given in the Table 2.

Voltage Range (V)	C_{JO} (pF)	M	V_J (V)	C_P (pF)
0–2.5	22.5	2.0	4.00	0.00
2.5–6.5	21.0	25.0	68.00	0.00
6.5–11	20.0	7.3	14.00	0.90
11–up	20.0	1.8	1.85	0.56

Table 2. Varactor Voltages

These subranges are made to overlap each other. Thus, if a reasonable RF swing (one that is appropriate in a practical VCO case) exceeds limits of the subrange, the C_V function described by the current subrange will still fit in the original curve.

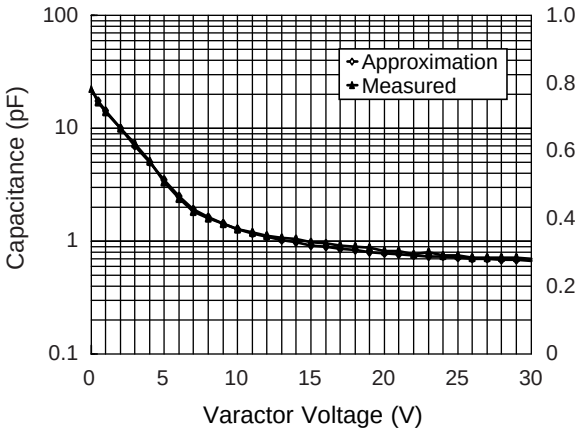

Figure 6. SMV1265 Capacitance vs. Voltage

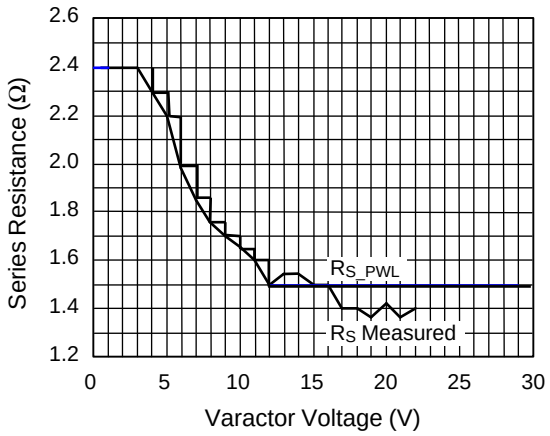

Figure 7. SMV1265 Resistance vs. Voltage

Figure 6 demonstrates the quality of the piece-wise fitting approach.

Special consideration was given to the fit at the lowest capacitance range (high-voltage area) since it dramatically affects the upper frequency limit of the VCO.

To incorporate this function into Libra, the pwl() built-in function was used in the “variables” component of the schematic bench.

M = pwl (V_{VAR} 0 2 2.5 2 2.500009 25 6.5 25 6.50009 7.3 11 7.3 11.0009 1.8 40 1.8)

V_J = pwl (V_{VAR} 0 4 2.5 4 2.500009 68 6.5 68 6.50009 14 11 14 11.0009 1.85 40 1.85)

C_P = pwl (V_{VAR} 0 0 2.5 0 2.500009 0 6.5 0 6.50009 0.9 11 0.9 11.0009 0.56 40 0.56)

C_{JO} = pwl (V_{VAR} 0 22.5 2.5 22.5 2.500009 21 6.5 21 6.50009 20 11 20 11.0009 20 40 20)*10^{12}

Note: While C_P is given in picofarads, C_{GO} is given in farads to comply with the default nominations in Libra. (For more details regarding pwl() function see Circuit Network Items, Variables and Equations, Series IV Manuals, p. 19–15).

Since the epitaxial layer for this kind of hyperabrupt varactor has relatively high resistivity the series resistance is strongly dependent on the reverse voltage applied to varactor junction. The value of series resistance (R_S) measured at 500 MHz is shown in Figure 7, with a piece-wise approximation of R_S also given.

The piece-wise function may be used as follows:

R_S = pwl (V_{VAR} 0 2.4 3 2.4 4 2.3 5 2.2 6 2 7 1.85 8 1.76 9 1.7 10 1.65 11 1.61 12 1.5 40 1.5)

Note: The pwl() function in Libra IV is defined for the evaluation of harmonic balance parameters rather than variables. Therefore, although series resistance was defined as dependent on reverse voltage, for harmonic balance it remains parametric and linear. The same applies to capacitance, which remains the same as in the original diode model, but its coefficients (V_J, M, C_{JO}, and C_P) become parametric functions of the reverse voltage.

VCO Design and Performance

Figure 8 shows the VCO schematic.

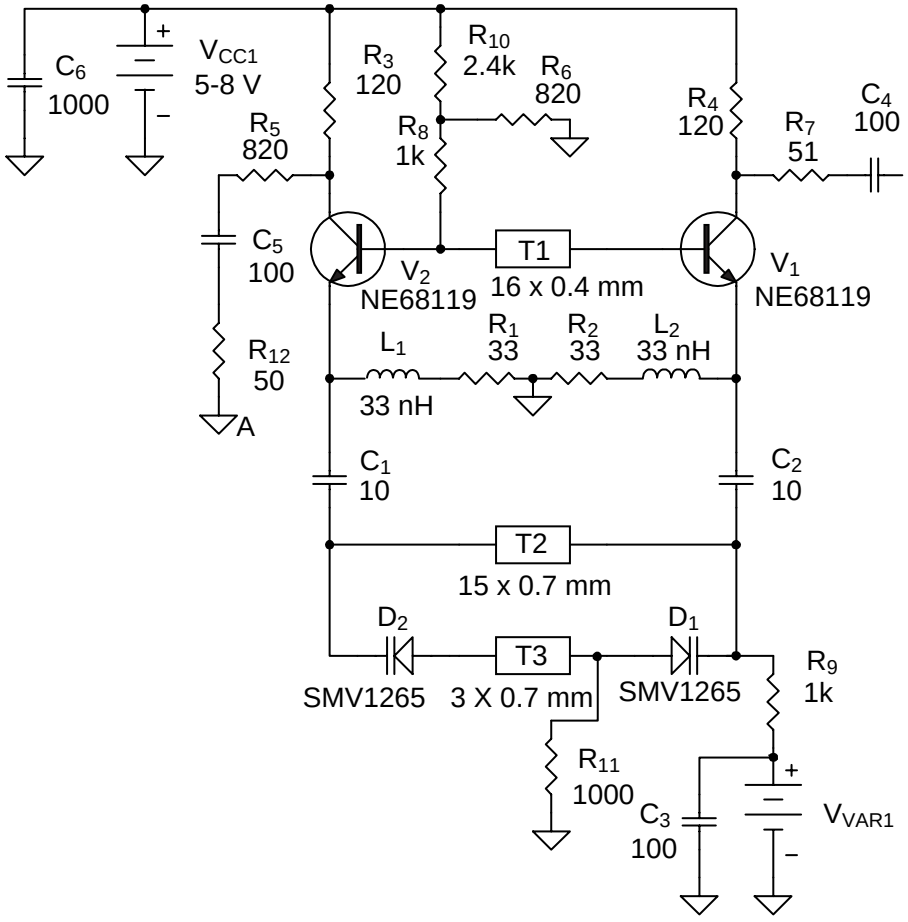

Figure 8. VCO Schematic

Table 3 shows the bill of materials used.

Designators	Comment	Footprint
C_1	0603AU100JAT9 (AVX)	0603
C_2	0603AU100JAT9 (AVX)	0603
C_3	0603AU101JAT9 (AVX)	0603
C_4	0603AU101JAT9 (AVX)	0603
C_5	0603AU101JAT9 (AVX)	0603
C_6	0603AU102JAT9 (AVX)	0603
C_6	0603AU102JAT9 (AVX)	0603
D_1	SMV1265-011 (Alpha Ind.)	SOD-323
D_2	SMV1265-011 (Alpha Ind.)	SOD-323
L_1	LL1608-F33NJ (TOKO)	0603
L_2	LL1608-F33NJ (TOKO)	0603
R_1	CR10-330J-T (AVX)	0603
R_{10}	CR10-242J-T (AVX)	0603
R_{11}	CR10-102J-T (AVX)	0603
R_2	CR10-330J-T (AVX)	0603
R_3	CR10-121J-T (AVX)	0603
R_4	CR10-121J-T (AVX)	0603
R_5	CR10-821J-T (AVX)	0603
R_6	CR10-821J-T (AVX)	0603
R_7	CR10-510J-T (AVX)	0603
R_8	CR10-102J-T (AVX)	0603
R_9	CR10-102J-T (AVX)	0603
V_1	NE68119 (NEC)	SOT-416
V_2	NE68119 (NEC)	SOT-416

Table 3. Bill of Materials

Figure 9 shows the PCB layout. The board is made of standard FR4 material 30 mils thick.

The results measured with the circuit in Figure 8, as well as the simulated results obtained with the model in Figure 9, are shown in Figures 10 and 11.

Note: The simulated tuning curve in Figure 10 agrees with measured data, which proves the effectiveness of the above piece-wise approximation technique.

Note: In the middle of the tuning range there is disagreement between our model and the measured results. This could be attributed to the imperfection of the model, which is highly sensitive to the way different parasitic effects are treated. The other problem of modeling this oscillator case was the convergence of the harmonic balance. To facilitate convergence in this case, we kept the number of harmonics to at least five. The sweeping frequency range is recommended to keep as close to the oscillation point as possible — especially when analyzing the middle band area.

In Figure 11, the power response modeled at 7 V was very close to the measurement. Higher measured power is attributed to the analyzer calibration (the calibration error of the analyzer is known to be within a couple of decibels). The general trend of the simulated results reflects the real VCO response almost exactly, which clearly demonstrates the model's effectiveness.

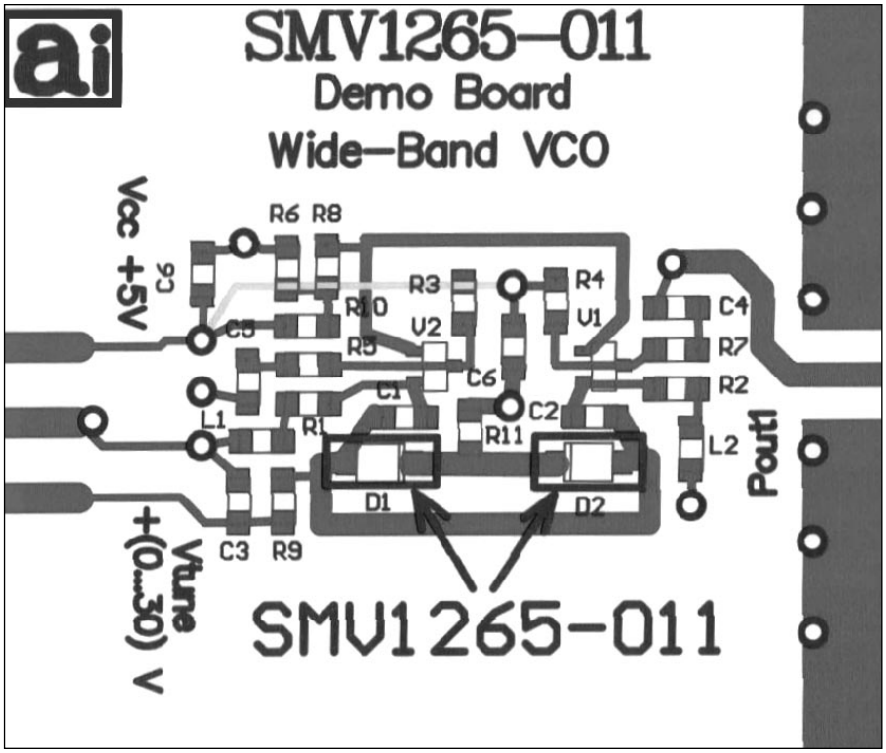

Figure 9. PCB Layout

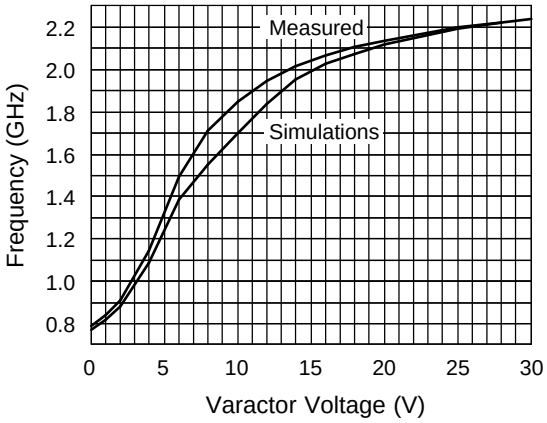

Figure 10. Frequency Tuning

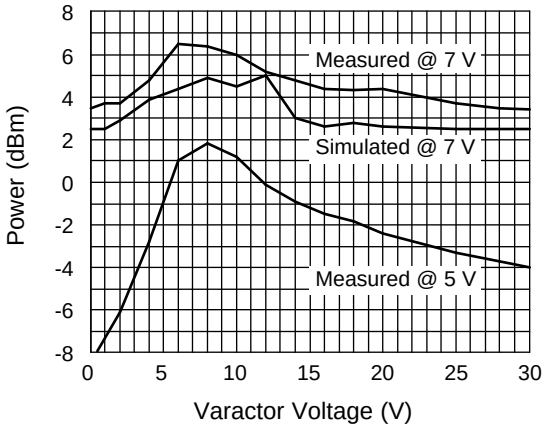

Figure 11. Power Response

Table 4 shows the measurement data and shows a useful tuning range of from 0.84–2.23 GHz for the applied varactor voltage from 1–27 V.

V_{VAR} (V)	Frequency (GHz)	P_{OUT} @ 7 V (dBm)	P_{OUT} @ 5 V (dBm)
0	0.788	3.5	-8.3
1	0.842	3.7	-7.6
2	0.91	3.7	-6.1
4	1.144	4.8	-2.8
6	1.492	6.5	1.0
8	1.714	6.4	1.8
10	1.848	6.0	1.2
12	1.946	5.2	-0.1
14	2.016	4.8	-0.9
16	2.066	4.4	-1.5
18	2.106	4.3	-1.8
20	2.134	4.4	-2.4
25	2.198	3.7	-3.3
28	2.225	3.5	-3.7
30	2.238	3.4	-4.0

Table 4. Tabulated Measurement Data

List of Available Documents

1. Balanced Wideband VCO Simulation Project Files for Libra IV.
2. Balanced Wideband VCO Circuit Schematic and PCB Layout for Protel EDA Client, 1998 version.
3. Balanced Wideband VCO Gerber Photo-plot Files
4. Detailed measurement and simulation data.

For the availability of the listed materials, please call our applications engineering staff.