

# A Low Phase Noise VCO Design for PCS Handset Applications



APN1016

## Introduction

The VCO design in a PCS handset must satisfy a number of stringent electrical, cost, and size requirements which include:

- Power supply
  - 3 V DC power supply
  - < 6 mA total current consumption
- Layout
  - Minimum components count
  - Aggressive PCB layout design and component placement rules with spacing less than 5 mils and placement pads no larger than component's land area
  - Total VCO footprint smaller than 7 x 8 mm
- Cost
  - Minimum component cost
  - Maximum production yield
  - Tight component tolerance control to minimize or avoid trimming
  - Total VCO cost well under \$0.50

The factors that have significant impact on the primary VCO electrical specifications may be summarized as follows:

- Primary design criteria
  - Frequency tuning range
  - Tuning sensitivity
  - Output power level
- Stability and spectrum purity factors
  - Phase noise at a given frequency offset
  - Frequency pulling when terminated with SWR > 2 at all phases
  - Frequency pushing
  - Temperature stability

Other electrical specifications may include harmonic content or spur levels in the output signal, tuning linearity, etc. However, for the existing handset VCO market these specifications have been standardized based on available technology. Some typical PCS VCO characteristics for PCS handsets are given in Table 1.

Parameter	Test Conditions	Manufacturer		
		Murata		Other
		MQE523	MQE920	Typical
Frequency Range* (GHz)	$V_{CTL} = 0.5 \text{ V}$	1.715	1.948	-
	$V_{CTL} = 2.5 \text{ V}$	1.778	2.086	-
Tuning Sensitivity (MHz/V)		31.5	69	40
Supply Voltage (V)		3	3	3
Supply Current (mA)		15.3	7	< 8
Control Voltage (V)	$V_{CTL}$	0.5–2.5	0.5–2.5	0.5–2.5
Output Power (dBm)	$P_{OUT}$	-2	-0.5	0
Pushing Figure (MHz/V)		3.8	-	< 2
Pulling Figure (MHz)	SWR = 2, for all phases	0.90	-	< 2
Phase Noise (dBc/Hz)	@ 10 kHz	-91	-91	-90

\*Frequency selection depends on the system requirement.

**Table 1. Typical Characteristics for PCS Handset VCOs**

This application note describes the design and performance of a VCO centered at 1750 MHz for a PCS handset that uses Alpha's SMV1763-079 varactor diode. This low R varactor was designed specifically for low phase noise applications. The VCO was designed to satisfy the listed requirements for a PCS handset.

### The Colpitts VCO Fundamentals

The fundamental Colpitts VCO operation is illustrated in Figures 1a and 1b.

Figure 1a shows a Colpitts VCO circuit the way it is usually implemented on a PCB. Figure 1b reconfigures the same circuit as a common-emitter amplifier with parallel feedback. We have separated the transistor junction and package capacitors,  $C_{EB}$ ,  $C_{CB}$  and  $C_{CE}$ , from the transistor parasitic components to demonstrate their direct effect on the VCO tank circuit.

In an actual low noise VCO circuit, the capacitor we noted as  $C_{VAR}$  may have a more complicated structure. It would include series and parallel connected discrete capacitors used to set the oscillation frequency and tuning sensitivity. The parallel connection of the resonator inductor,  $L_{RES}$ , and the varactor capacitive branch,  $C_{VAR}$ , refer to the

parallel resonator (or simply resonator). A fundamental property of the parallel resonator in a Colpitts VCO implementation is its inductive impedance at the oscillation frequency. This means that its parallel resonant frequency is always higher than the oscillation frequency.

At parallel resonance in the resonator branch, the impedance in the feedback loop is high, acting like a stop-band filter. Thus, the closer the oscillation frequency to the parallel resonant frequency, the higher the loss introduced in the feedback path. However, since more reactive energy is stored in the parallel resonator closer to the resonant frequency, then higher  $Q_L$  will be achieved. Obviously, low loss resonators, like crystal or dielectric resonators, allow much closer and lower oscillation loss buildup at parallel resonance, in comparison to microstrip or discrete inductor-based resonators.

The proximity of the parallel resonance to the oscillation frequency may be effectively established by the  $C_{SER}$  capacitor value. Indeed, if the capacitance of  $C_{SER}$  is reduced, the parallel resonator will have higher inductance to compensate for the increased capacitive reactance. This means that the oscillation frequency will move closer to parallel resonance resulting in higher  $Q_L$  and higher feedback loss.

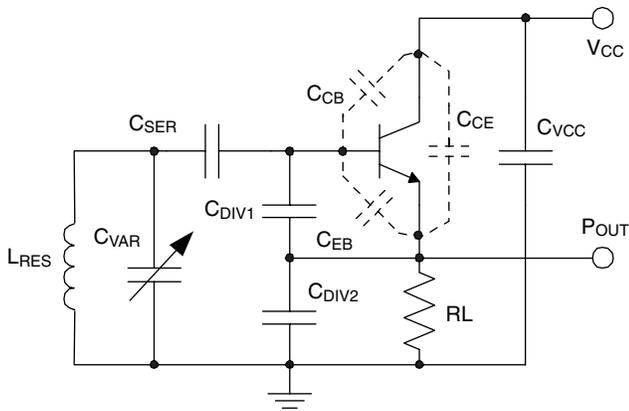


Figure 1a. Basic Colpitts VCO Configuration

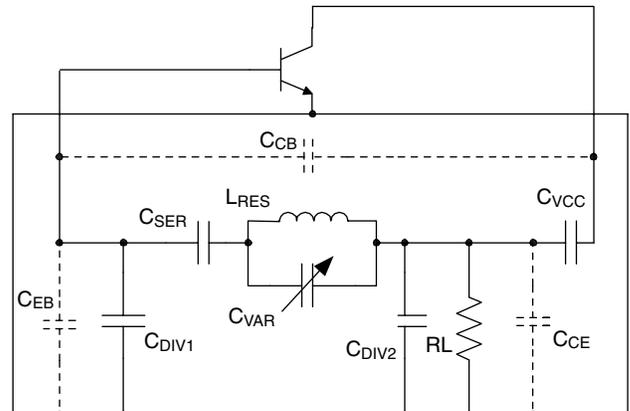


Figure 1b. Common-Emitter View of the Colpitts VCO

The Leeson equation, establishing a connection between tank circuit  $Q_L$  and its losses, states:

$$\xi(f_m) = \frac{FkT}{2P} \left( 1 + \frac{f^2}{4Q_L^2 f_m^2} \right)$$

Where F is the large signal noise figure of the amplifier as shown in Figure 1b; P is the loop or feedback power (measured at the input of the transistor); and  $Q_L$  is loaded Q. These three parameters have significant consequences for phase noise in an actual low noise RF VCO. In designing a low noise VCO, we need to define the condition for minimum F and maximum P and  $Q_L$ .

This discussion shows that loop power and  $Q_L$  are contradictory parameters. That is, an increase in  $Q_L$  leads to more loss in the feedback path resulting in lower loop power. The condition for the optimum noise figure is also contrary to maximum loop power and largely depends on the specific transistor used. The best noise performance is usually achieved with a high gain transistor and the maximum gain coinciding with minimum noise at large

signals. Since there are no such specifications currently available for standard industry transistors, we can only base our transistor choice on experience.

### The VCO Model

In Figure 2, the transistors  $X_1$  and  $X_2$  are connected in DC Cascode sharing the base biasing network consisting of  $R_2$  ( $R_{DIV1}$ ),  $R_3$  ( $R_{DIV2}$ ) and  $R_4$  ( $R_{DIV3}$ ). The bias resistor values were designed to distribute the DC voltages evenly between  $X_1$  and  $X_2$ . Resistor  $R_6$  ( $R_L$ ) was chosen as low as 100 to minimize the DC voltage drop to the specified 8 mA. At RF frequencies,  $X_2$  works as a common-emitter amplifier with the emitter grounded through capacitor SRLC2. The oscillator stage output is fed to the buffer transistor through coupling capacitor  $C_{17}$  ( $C_{CPL}$ ).

The output circuit of the buffer stage consists of the printed microstrip-line inductor  $TL_5$  and output capacitor  $C_1$  ( $C_{OUT}$ ). Capacitor SLC2, in parallel with the microstrip-line inductor  $TL_5$ , may be used for finer trimming, when SLC2 is selected lower than 0.5 pF.

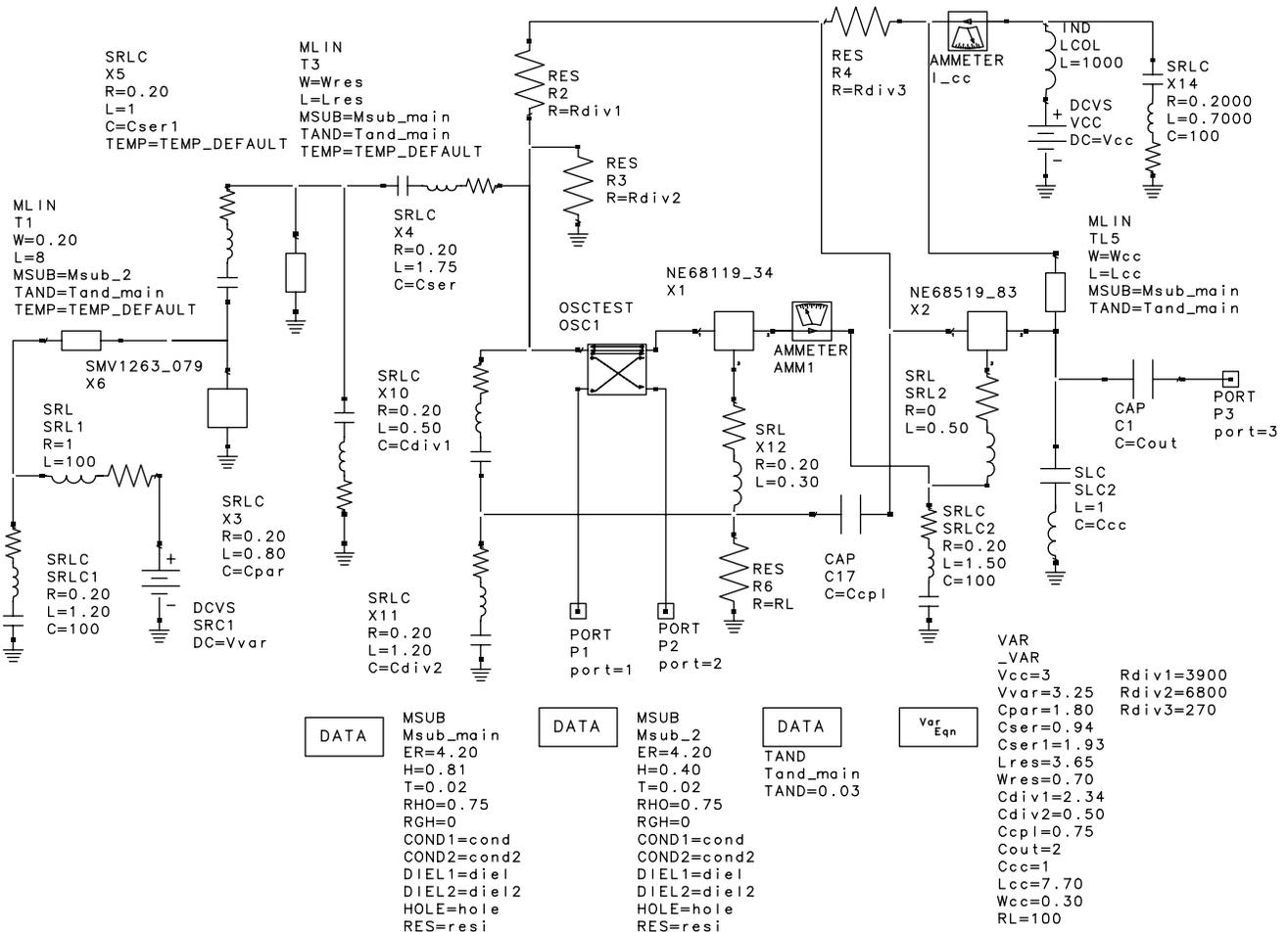


Figure 2. PCS VCO Schematic for Libra IV, Using DC Cascode Colpitts VCO Configuration

The resonator circuit consists of the printed microstrip-line inductor  $T_3$  in parallel with ceramic capacitor  $X_3$  ( $C_{PAR}$ ), the capacitive varactor branch with  $X_5$  ( $C_{SER1}$ ) and varactor SMV1763-079  $X_6$  connected in series. The model for varactor SMV1763-079 is described in a separate circuit schematic bench shown in Figure 4. The varactor choice was based on the VCO frequency coverage and the requirement for low phase noise. This requirement is related to the need for low equivalent series resistance,  $R_{S\_EQV}$ , in the overall VCO resonator.

The equivalent series resistance of the capacitive branch of the VCO resonator, shown in Figure 1, includes the varactor with its series resistance. This resistance may be expressed as follows:

$$R_{S\_EQV} \approx K_V K_f (R_S + r_S + r_P) \frac{C_{JO}}{C_E} - 2r_P \sqrt{K_V K_f \frac{C_{JO}}{C_E} + r_P}$$

Where:

$$K_V = 2 \frac{V_J}{M} \left(1 + \frac{V_{VAR}}{V_J}\right)^{1-M}; K_f = \frac{1}{f} \frac{\Delta f}{\Delta V_{VAR}}$$

$V_{VAR}$  is the varactor DC bias in the middle of the tuning range;

$C_E$  is the capacitance of the resonator capacitive branch in the middle of the tuning range;

$C_{JO}$ ,  $V_J$ ,  $M$  are the parameters describing varactor capacitance<sup>[1]</sup>;

$R_P$ ,  $R_S$  are the series resistances of  $C_{PAR}$  and  $C_{SER1}$ ; and

$K_F$  is the relative tuning sensitivity.

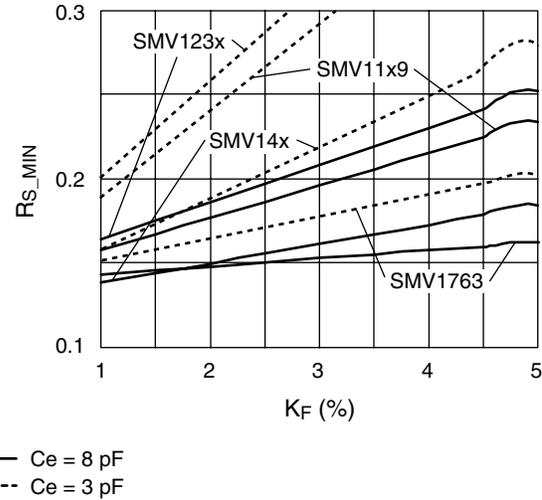


Figure 3. Optimum  $R_S$  vs. Relative Frequency Sensitivity for Different  $C_E$

The results of this equation versus relative tuning sensitivity are given in Figure 3 for different varactor processes. The low resistance SMV1763 process looks best for tuning sensitivities higher than 1.5–2.0% per V.

The values of variables used in the circuit are given in the variable equation module.

The default and test benches are shown in Figures 4 and 5 respectively.

```

[UNIT]
UNITS
UNITS_DEFAULT
FREQ=GHz
RES=Ohm
COND=S
IND=nH
CAP=pF
LNG=mm
TIME=psec
ANG=deg
POWER=dBm
VOLT=V
CUR=mA
DIST=mi

[DATA]
MSUB
MSUB_DEFAULT
ER=10
H=25
T=0.15
RHO=1
RGH=0
COND1=cond
COND2=cond2
DIEL1=die1
DIEL2=die12
HOLE=hole
RES=resi

[DATA]
DATA
TEMP
TEMP_DEFAULT
TEMP=27

[DATA]
DATA
TAND
TAND_DEFAULT
TAND=0

[DATA]
DATA
RREF
RREF_DEFAULT
R=50

[VAR]
VAR
VAR
VAR
Power=-8.50
    
```

Figure 4. Default Bench for Libra IV

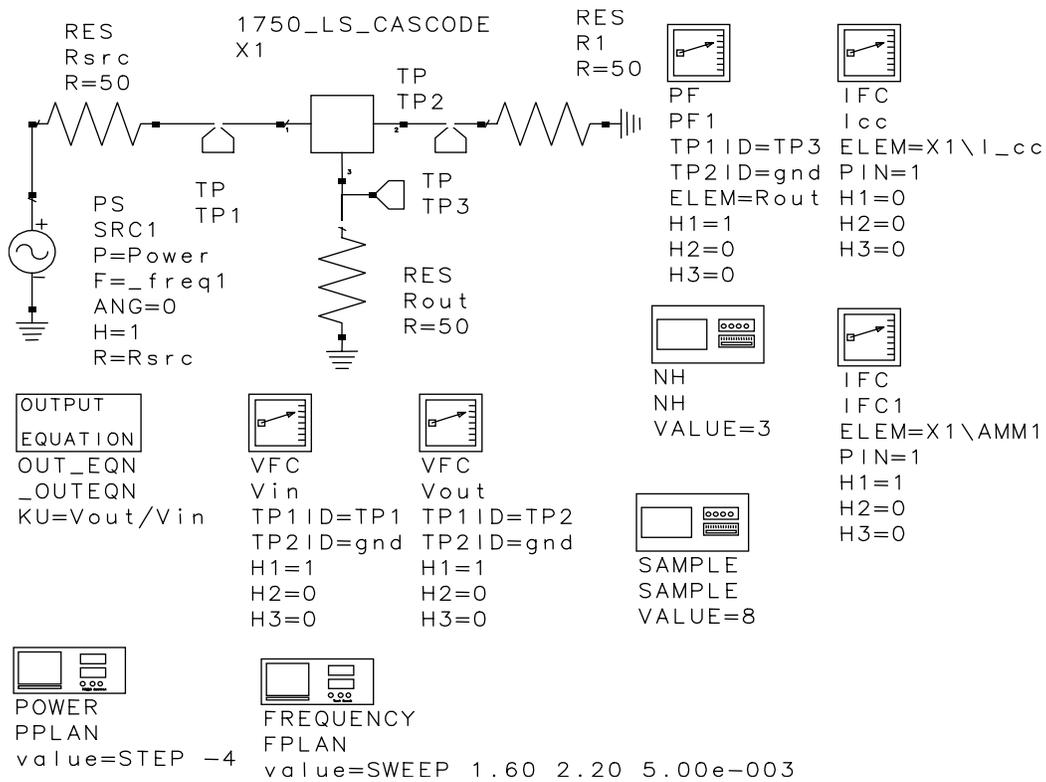


Figure 5. PCS VCO Test Bench

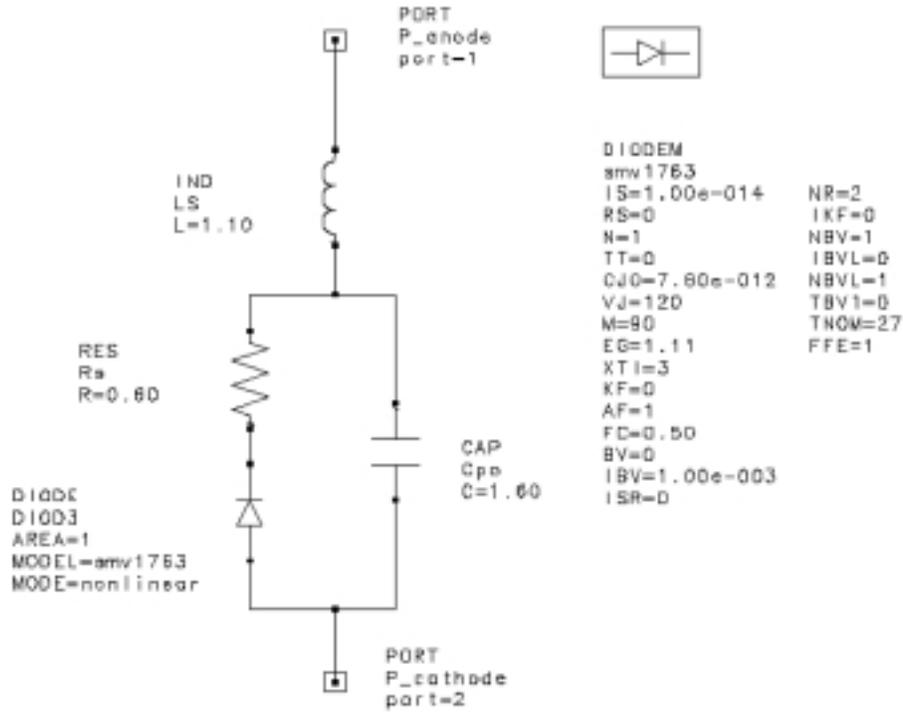


Figure 6. SMV1763-079 SPICE Model for Libra IV

### SMV1763-079 SPICE Model

The SMV1763-079 is a low series resistance, hyperabrupt varactor diode. It has the industry’s smallest plastic package, SC-79, with a body size of 47 x 31 x 24 mils (total length with leads is 62 mils).

The SPICE model for the SMV1763-079 varactor diode, defined for the Libra IV environment, is shown in Figure 6 with a description of the parameters employed.

Table 2 describes the model parameters. It shows default values appropriate for silicon varactor diodes that may be used by the Libra IV simulator.

Parameter	Description	Unit	Default
IS	Saturation current (with N, determine the DC characteristics of the diode)	A	1e-14
R <sub>S</sub>	Series resistance	Ω	0
N	Emission coefficient (with IS, determines the DC characteristics of the diode)	-	1
TT	Transit time	S	0
C <sub>JO</sub>	Zero-bias junction capacitance (with V <sub>J</sub> and M define nonlinear junction capacitance of the diode)	F	0
V <sub>J</sub>	Junction potential (with V <sub>J</sub> and M define nonlinear junction capacitance of the diode)	V	1
M	Grading coefficient (with V <sub>J</sub> and M define nonlinear junction capacitance of the diode)	-	0.5
E <sub>G</sub>	Energy gap (with XTI, helps define the dependence of IS on temperature)	EV	1.11
XTI	Saturation current temperature exponent (with E <sub>G</sub> , helps define the dependence of IS on temperature)	-	3
KF	Flicker-noise coefficient	-	0
AF	Flicker-noise exponent	-	1
FC	Forward-bias depletion capacitance coefficient	-	0.5
B <sub>V</sub>	Reverse breakdown voltage	V	Infinity
I <sub>BV</sub>	Current at reverse breakdown voltage	A	1e-3
ISR	Recombination current parameter	A	0
NR	Emission coefficient for ISR	-	2
IKF	High-injection knee current	A	Infinity
NBV	Reverse breakdown ideality factor	-	1
IBVL	Low level reverse breakdown knee current	A	0
NBVL	Low level reverse breakdown ideality factor	-	1
T <sub>NOM</sub>	Nominal ambient temperature at which these model parameters were derived	°C	27
FFE	Flicker-noise frequency exponent	-	1

**Table 2. Silicon Diode Default Values in Libra IV**

According to the SPICE model, the varactor capacitance, C<sub>V</sub>, is a function of the applied reverse DC voltage, V<sub>R</sub>, and may be expressed as follows:

$$C_V = \frac{C_{JO}}{\left(1 + \frac{V_R}{V_J}\right)^M} + C_P$$

This equation is a mathematical expression of the capacitance characteristic. This model is accurate for abrupt junction varactors (like Alpha’s SMV1408); however, for hyperabrupt junction varactors the model is

less accurate because the coefficients are dependent on the applied voltage. To make the equation work better for the hyperabrupt varactors the coefficients were optimized for the best capacitance versus voltage fit, as shown in Table 3.

Please note that in the Libra model above, C<sub>P</sub> is given in picofarads, while C<sub>JO</sub> is given in farads to comply with the default unit system used in Libra.

Part Number	C <sub>JO</sub> (pF)	M	V <sub>J</sub> (V)	C <sub>P</sub> (pF)	R <sub>S</sub> (Ω)	L <sub>S</sub> (nH)
SMV1763-079	7.6	90	120	1.6	0.6	1.1

**Table 3. SPICE Parameters for SMV1763-079**

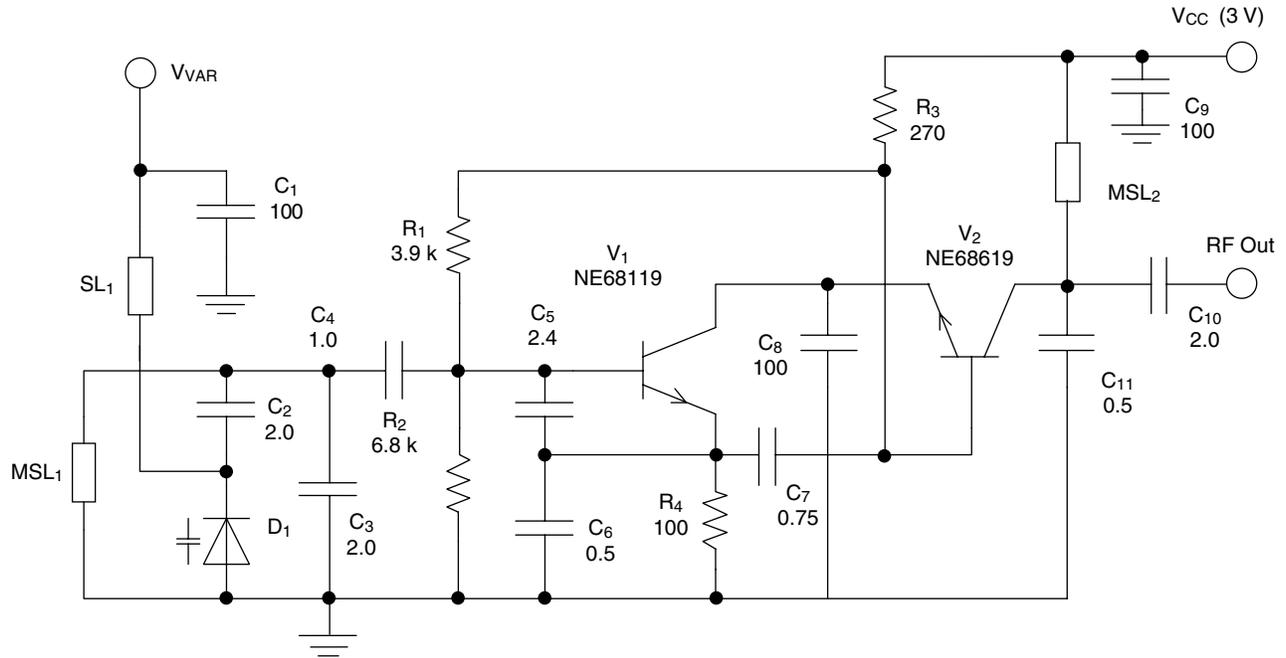


Figure 7. PCS VCO Schematic (D<sub>1</sub>: SMV1763-079)

### VCO Design, Materials and Layout

The VCO schematic diagram is shown in Figure 7. The circuit is powered by a 3 V voltage source. The I<sub>CC</sub> current was established near 8 mA. The RF output signal is coupled from the VCO through the capacitor C<sub>10</sub> (2 pF).

The PCB layout is shown in Figure 8. The board was made of standard, 30 mil thick FR4 material. A more detailed drawing of the VCO layout is shown in Figure 9 with the dimensions of critical circuit components.

The bill of materials used is given in Table 4.

Designator	Value	Part Number	Footprint	Manufacturer
C <sub>1</sub>	100 p	0402AU101KAT	0402	AVX
C <sub>2</sub>	2 p	0402AU2R0JAT	0402	AVX
C <sub>3</sub>	2 p	0402AU2R0JAT	0402	AVX
C <sub>4</sub>	1 p	0402AU1R0JAT	0402	AVX
C <sub>5</sub>	2.4 p	0402AU2R4JAT	0402	AVX
C <sub>6</sub>	0.5 p	0402AU0R5JAT	0402	AVX
C <sub>7</sub>	0.75 p	0402AU0R75JAT	0402	AVX
C <sub>8</sub>	100 p	0402AU101KAT	0402	AVX
C <sub>9</sub>	100 p	0402AU101KAT	0402	AVX
C <sub>10</sub>	2 p	0402AU2R0KAT	0402	AVX
C <sub>11</sub>	0.5 p	0402AU0R5KAT	0402	AVX
D <sub>1</sub>	SMV1763-079	SMV1763-079	SC-79	Alpha Ind.
R <sub>1</sub>	3.9 k	CR10-392J-T	0402	AVX/KYOCERA
R <sub>2</sub>	6.8 k	CR10-682J-T	0402	AVX/KYOCERA
R <sub>3</sub>	270	CR10-271J-T	0402	AVX/KYOCERA
R <sub>4</sub>	100	CR10-101J-T	0402	AVX/KYOCERA
V <sub>1</sub>	NE68119	NE68119	SOT-416	NEC/CEL
V <sub>2</sub>	NE68619	NE68619	SOT-416	NEC/CEL

Table 4. Bill of Materials

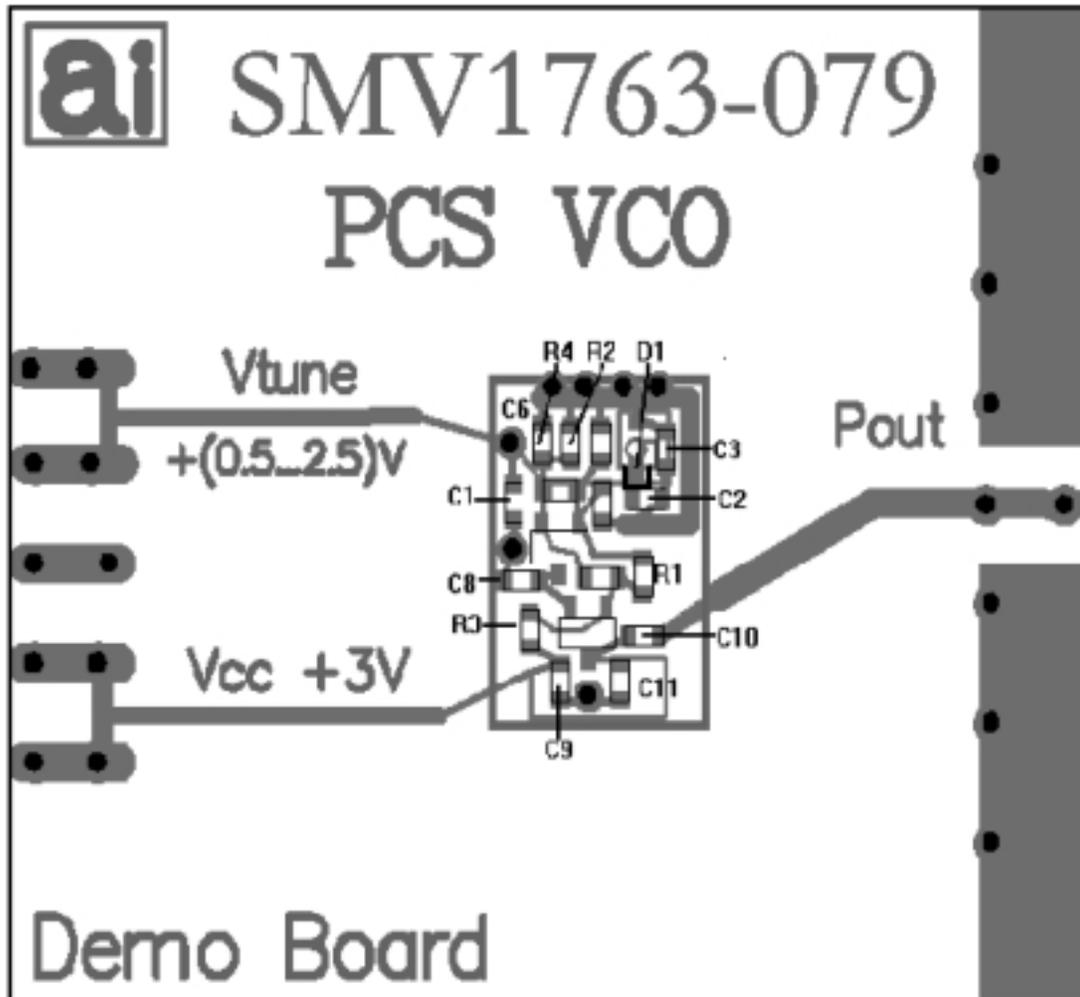


Figure 8. PCB Layout

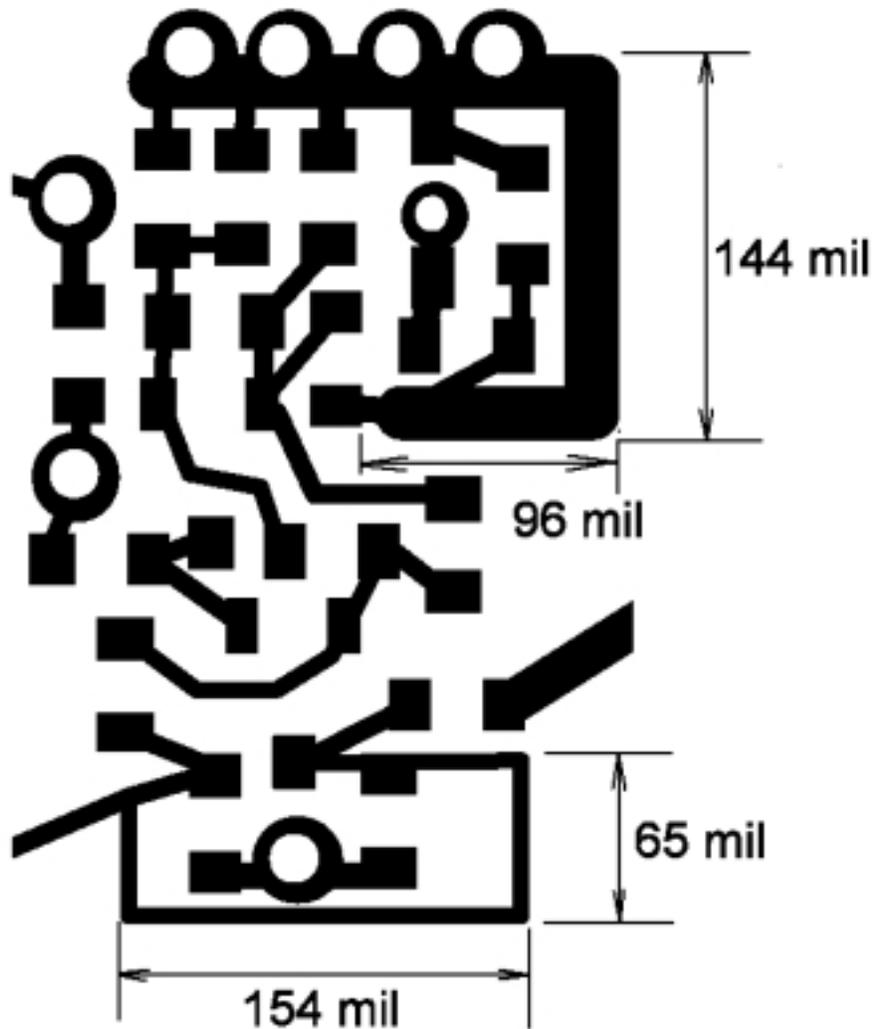


Figure 9. Detailed Drawing of the PCS VCO Layout

## Measurement and Simulation Results

The measured performance of this circuit and the simulated results obtained with the model are shown in Figures 10 through 12. Phase noise measurements versus frequency offset are shown in Figure 12. It shows greater than  $-90$  dBc/Hz at 10 kHz offset and greater than  $-110$  dBc/Hz at 100 kHz offset. This 20 dB/decade slope is fairly constant up to 5–6 MHz. The measurements were done in the range below 7 MHz, offset because of the 100 ns delay-line setup used. This measurement was made using the Aeroflex PN9000 Phase Noise Test Set.

The measured frequency tuning response in Figure 10 shows linear 60 MHz/V tuning in the 0.5–2.5 V range typical for battery applications. The simulated frequency tuning response is very similar to the measured response. VCO output power variation versus tuning shows a divergence within  $\pm 2$  dB between measurement and simulation. This may be attributed to the VCO model parameters, especially to the transistor model parameters. These models are usually derived for small signal amplifier applications, and may not necessary reflect the higher non-linearity of a VCO.

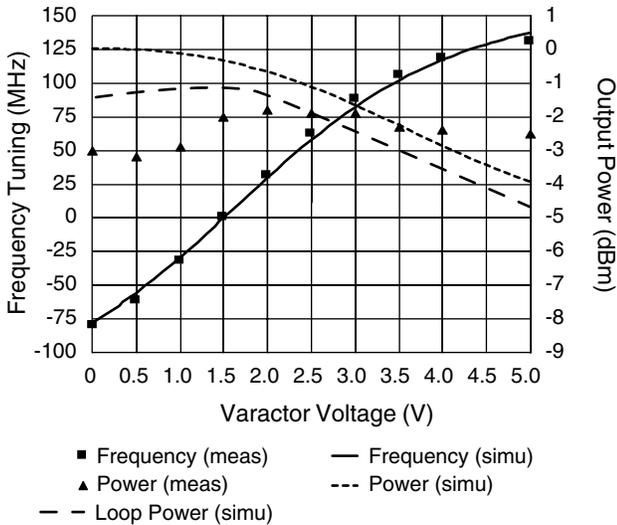


Figure 10. Tuning Response Centered at 1750 MHz for  $V_{CC} = 3\text{ V}$ ,  $V_{VAR} = 1.5\text{ V}$

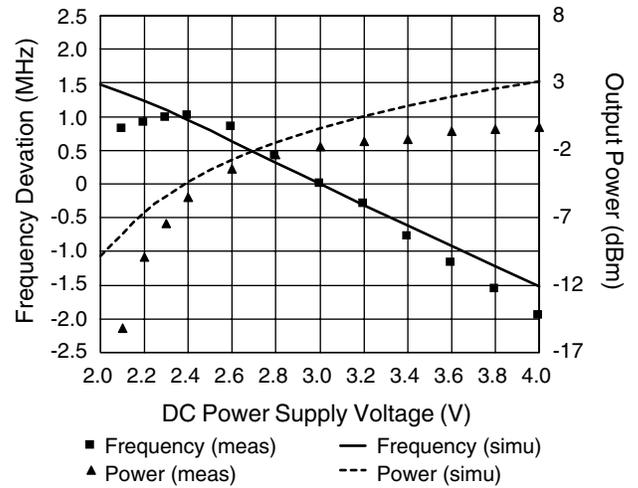


Figure 11. DC Supply Pushing Response Centered at 1750 MHz for  $V_{CC} = 3\text{ V}$ ,  $V_{VAR} = 1.5\text{ V}$

The simulated loop power shows constant behavior in the battery range of 0.5–2.5 V and rapid degradation above it. This degradation may cause proportional degradation of phase noise according to the Leeson equation.

The DC supply pushing response, shown in Figure 11, shows even larger differences between simulated and measured data. The measured “slow down” of pushing

near 2.4 V indicates that pushing in the VCO may be further minimized by reducing the DC bias current. However, the model supplied by the transistor vendor does not reflect a negative pushing slope. The simulation results shown in Figure 11 were obtained for a modified transistor model, which is available with the PCS VCO simulation project file.

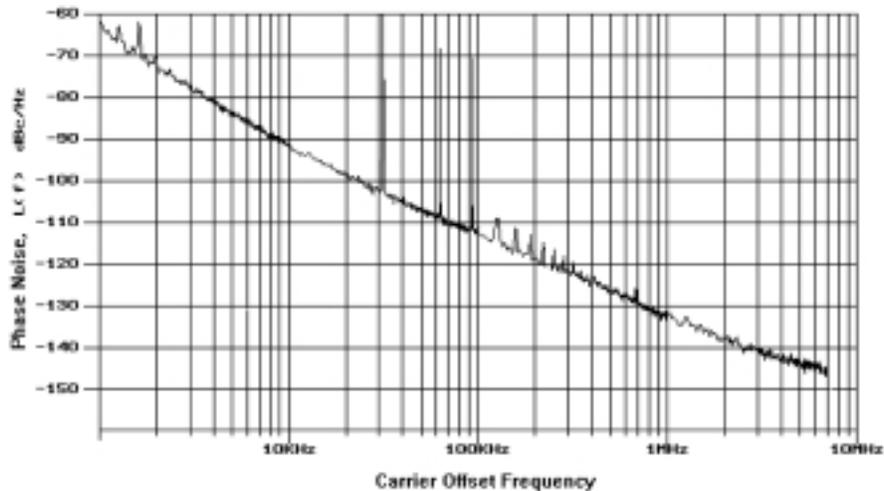


Figure 12. Measured Phase Noise at 1750 MHz for  $V_{CC} = 3\text{ V}$ ,  $V_{VAR} = 1.5\text{ V}$

## List of Available Documents

The PCS VCO Simulation Project Files for Libra IV.

The PCS VCO Circuit Schematic and PCB Layout for Protel, EDA Client, 1998 version.

The PCS VCO PCB Gerber Photo-plot Files.

## VCO Related Application Notes

APN1004, Varactor SPICE Models for RF VCO Applications.

APN1006, A Colpitts VCO for Wide Band (0.95 GHz–2.15 GHz) Set-Top TV Tuner Applications.

APN1005, A Balanced Wide Band VCO for Set-Top TV Tuner Applications.

APN1007, Switchable Dual-Band 170/420 MHz VCO for Handset Cellular Applications.

APN1012, VCO Designs for Wireless Handset and CATV Set-Top Applications.

APN1013, A Differential VCO for GSM Handset Applications.